MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018

EEE3196 – INTEGRATED VLSI SYSTEMS

(EE)

7 MARCH 2018
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This examination paper consists of 7 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Formulas:

Ideal diode equation: $I_D = I_S(e^{\frac{V_D}{\Phi T}} - 1)$

$$V_T = V_{TO} + \gamma(\sqrt{|-2\emptyset_F + V_{SB}|} - \sqrt{|-2\emptyset_F|})$$

saturation:

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

linear:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{{V_{DS}}^2}{2}\right)$$

unified model:

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DSAT} - \frac{{V_{DSAT}}^2}{2}\right)(1 + \lambda V_{DS})$$

$$t_P = \frac{C_L\frac{V_{SWING}}{2}}{I_{AVG}}$$

$$t_P = 0.69\,R_{eq}C_L$$

$$P_{dyn} = C_L{V_{DD}}^2 f$$

Question 1

(a) Given a CMOS inverter with the following parameters:
$k'_n = 80\ \mu A/V^2$, $k'_p = -30\ \mu A/V^2$, $V_{Tn} = |V_{Tp}| = 0.5$ V, $V_{DD} = 3$ V, $V_{GS} = 2.5$ V, $(W/L)n = 2$, $(W/L)p = 5$ and $C_L = 50$ fF.

(i) Calculate the current (I_d) of the NMOS transistor when it is operating at
- saturation region ($V_{out} = 3$ V), and
- linear region ($V_{out} = 1.5$ V)

[4 marks]

(ii) Using the average current (I_{avg}) method, find the high-to-low propagation delay (t_{PHL}).

[4 marks]

(iii) Using the average on-resistance (Ron) method, find the high-to-low propagation delay (t_{pHL}).

[4 marks]

(iv) Compare the answers for two different methods above in part (ii) and part (iii) and comment.

[2 marks]

(v) Find the low-to-high propagation delay (t_{PLH}) and the total propagation delay (t_p).

[4 marks]

(b) Figure Q1 shows the graph of Voltage Scaling against Technology Generation(μm).
(i) Critic and comment on the graph.
(ii) Based on the graph, predict the dynamic power consumption for technology at 0.065 μm and beyond.
(iii) Discuss TWO ways on how the power can be dissipated.

[2+1+4 marks]

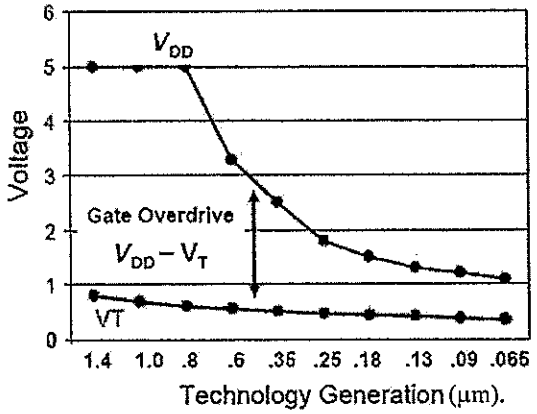


Figure Q1

Continued...

Question 2

(a) Consider a polysilicon line consisting of three segments (A, B, C), as shown in Figure Q2 below. Assume that the sheet resistance of the line is 30 Ω/square and the typical interwire capacitance values are:

Area capacitance = 0.058 fF/μm^2

Fringing capacitance = 0.043 fF/μm

(i) Calculate the total resistance with this line.

(ii) Calculate the total capacitance associated with this line.

(iii)Propose TWO methods to reduce the RC delay.

[5+6+4 marks]

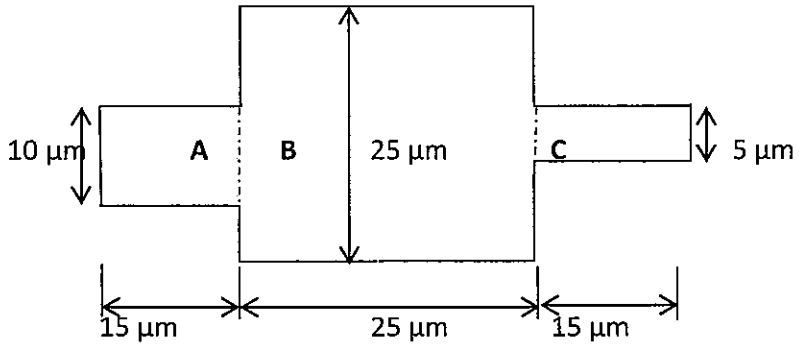


Figure Q2

(b) What are the common materials used for IC (Integrated Circuit) packaging? Describe the TWO bonding levels for packaging with the aid of diagrams.

[1+4 marks]

(c) Packaging is very important in the Integrated Circuit (IC) Industry. There are a few steps that could be taken to minimize overall chip power dissipation. Describe TWO steps for power minimization in chip.

[5 marks]

Continued...

Question 3

(a) Given the following function:

$$F = \overline{A + (B.C)}$$

(i) Design and sketch the circuit for this function F using conventional static CMOS transistors.

(ii) From part (i), modify the circuit F using the following methods:

a. dynamic logic

b. pseudo NMOS

(iii) Based on the modified design in part (ii), describe at least TWO advantages of using dynamic gates compared to pseudo NMOS.

[6+8+2 marks]

(b) There are a few techniques that can be used to design fast and complex logic gates for combinational logic design. Describe TWO design techniques.

[4 marks]

(c) Figure Q3 shows the circuit diagram of JK flip flop in which two AND gates are placed input to the SR flip flop.

(i) Describe the operation of this JK circuit when CLK goes HIGH.

(ii) Elaborate on step to avoid race condition in JK flip flop.

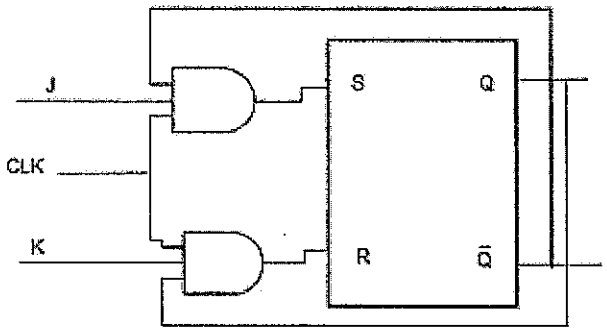


Figure Q3

[3+2 marks]

Continued...

Question 4

(a) Given a 16-bit ripple carry adder (RCA) with its t_{carry} = 200ps and t_{sum} = 300ps.

(i) Find the worst case delay t_{adder} .

(ii) Give an example of input values that will trigger this worst case delay.

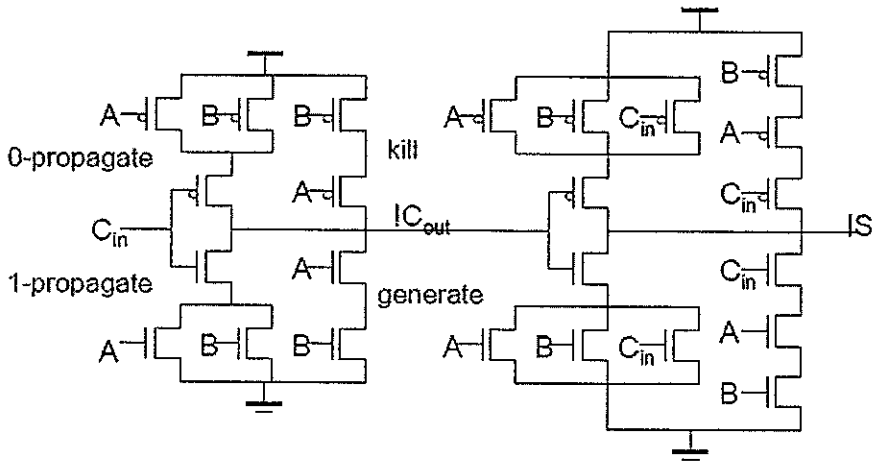
[3+2 marks]

(b) Figure Q4(a) shows a mirror adder circuit. It's known as a better structure for an adder which consists of 24 transistors.

(i) Describe the features in mirror adder which is not available in a static CMOS full adder.

(ii) Elaborate on TWO advantages of this mirror adder.

[6+4 marks]



C_{out} = A&B | B&C_{in} | A&C_{in} SUM = A&B&C_{in} | C_{OUT}&(A | B | C_{in})

Figure Q4(a)

Continued...

(c) Figure Q4(b) shows a Floating-gate Tunneling Oxide (FLOTOX) transistor.

(i) Describe the operation of this FLOTOX transistor.

(ii) Compare between a FLOTOX transistor and a floating-gate avalanche-injection MOS (FAMOS) transistor. Analyse at least TWO differences between them.

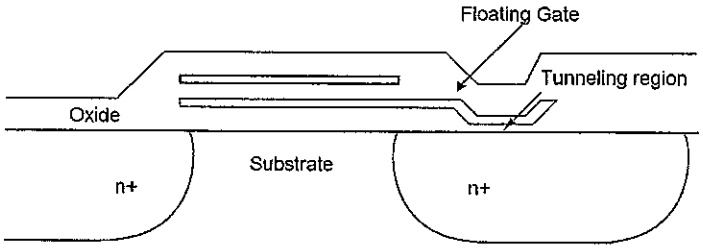
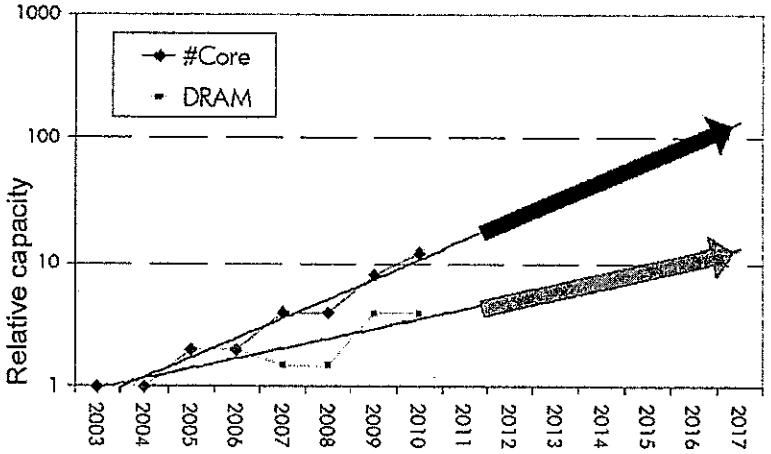


Figure Q4(b)

[2+4 marks]

(d) Figure Q4(d) shows the memory capacity gap. Comment on the graph especially on the memory capacity per core.



Source: Lim et al., ISCA 2009

Figure Q4(d)

[4 marks]

End of Paper